SPECIFICATION
FOR
EPD Module

MODULE No:	KD042HVFSN002
CUSTOMER:	

STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

Revision History

Date	Rev. No.	Page	Summary
2023.07.08	V1.0	ALL	FIRST ISSUE

Contents

1. Over View

KD042HVFSN002 is a 4.2" a-Si, active matrix TFT, Electronic Paper Display (EPD) panel. The panel is capable to show Black, White. The panel has high resolution (120dpi) that it is able to easily display fine patterns. Due to its bi-stable nature, the EPD panel requires very little power to update and needs no power to maintain an image.

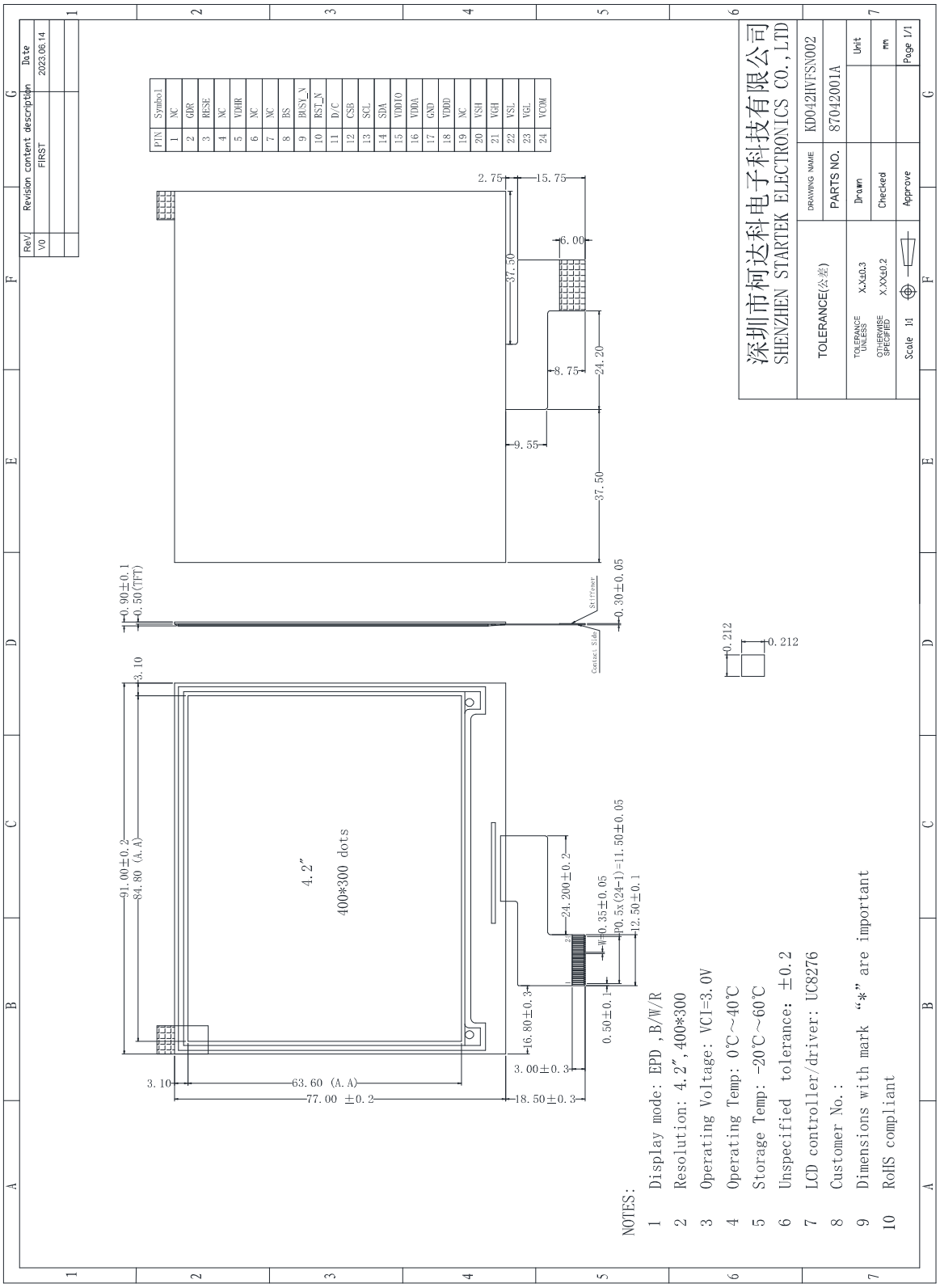
2. Features

- a-Si TFT active matrix Electronic Paper Display(EPD)
- Three colors support: White, Black, Red
- Resolution: 400 x 300
- Ultra-low power consumption
- Super Wide Viewing Angle - near 180° 1.2.6 Extra thin & light
- SPI interface
- RoHS compliant

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	4.2	Inch	
Display Resolution	400(H) x 300(V)	Pixel	
Active Area	84.8(H) x63.60(V)	mm	
Pixel pitch	0.212(H) x0.212(V)	mm	
Pixel Configuration	Vertical stripe		
Outline Dimension	91(H) x 77(V) x 0.9(D)	mm	
Module Weight	13	g	
Controller IC	UC8276		
Interface	3Wire / 4Wire SPI	-	
Display mode	EPD,B / W / R	-	
Operating temperature	0～+40	℃	
Storage temperature	-20～+60	℃	

4. Mechanical Drawing of EPD module



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常 备 库 存 Stock For Sale | 长 期 供 货 Long Time supply | 支持小量 NO MOQ | 品 种 齐 全 In Full Range

5. Input/Output Pin Assignment

NO.	Name	DISCRIPTION	I/O	Remark
1	NC	NO Connection	-	Keep open
2	GDR	N-Channel MOSFET Gate Drive Control	O	
3	RESE	Current Sense Input for the Control Loop	I	
4	NC	NO Connection	-	Keep open
5	VDHR	Positive Source driving voltage(Red)	C	
6	TSCL	IIC Interface to digital temperature sensor Clock pin	O	
7	TSDA	IIC Interface to digital temperature sensor Data pin	I/O	
8	BS	Bus Interface selection pin	I	Note 5-5
9	BUSY	Busy state output pin	O	Note 5-4
10	RES#	Reset signal input. Active Low.	I	Note 5-3
11	D/C#	Data /Command control pin	I	Note 5-2
12	CS#	Chip select input pin	I	Note 5-1
13	SCL	Serial Clock pin (SPI)	I	
14	SDA	Serial Data pin (SPI)	I/O	
15	VDDIO	Power Supply for interface logic pins It should be connected with VCI	P	
16	VDDA	Power Supply for the chip	P	
17	GND	Ground	P	
18	VDDD	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	C	
19	VPP	FOR TEST	P	
20	VSH	Positive Source driving voltage	C	
21	VGH	Power Supply pin for Positive Gate driving voltage and VSH1	C	
22	VSL	Negative Source driving voltage	C	
23	VGL	Power Supply pin for Negative Gate driving voltage VCOM and VSL	C	
24	VCOM	VCOM driving voltage	C	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output),
P = Power Pin, C =Capacitor Pin

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled Low.

Note 5-2: This pin (D/C#) is Data/Command control pin connecting to the MCU in 4 -wire SPI mode. When the pin is pulled High, the data at SDA will be interpreted as data. When the pin is pulled Low, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin High when –Outputting display waveform -Communicating with digital temperature sensor.

Note 5-5: This pin (BS) is for 3-line SPI or 4-line SPI selection. When it is "Low", 4-line SPI is selected. When it is "High", 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

BS State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{DD} V_{DDIO}	-0.3 to +6.0	V
Logic Input voltage	V_{IN}	-0.5 to V_{DD}+0.5	V
Logic Output voltage	V_{OUT}	-0.5 to V_{DD}+0.5	V

Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VDD=3.0V, T_{OPR} =25ºC

Parameter	Symbol	Conditions	Applicable pin	Min.	Typ.	Max	Units
Logic supply voltage	V_{DD},V_{DDIO}	-	VDD	2.3	3.0	3.6	V
High level input voltage	V_{IH}	-	-	0.7 V_{DDIO}	-	V_{DDIO}	V
Low level input voltage	V_{IL}	-	-	0	-	0.3V_{DDIO}	V
High level output voltage	V_{OH}	IOH = -400uA	-	V_{DDIO}-0.4	-	-	V
Low level output voltage	V_{OL}	IOL = 400uA	-	0	-	0.4	V
Typical power	P_{TYP}	-	-	-	-	-	mW
Deep sleep mode	P_{STPY}	-	-	-	-	-	mW
Typical operating current	Iopr_VDD	V_{dd} =3.0V	-	-	-	-	mA
Input Current （Mean）	I_{VCI}	-		-	4.93	-	mA
Input Current （Peak）	I_{VCI}	-		-	-	-	mA
Input Power	-	-		-	79.91	-	mA

Notes:1.The typical power consumption is measured with following pattern transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern.

2.The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

3.The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by SID.

6.3 AC Characteristics

6.3.1 MCU Interface selection

The pin assignment at different interface mode is summarized in Table.Different MCU mode can be set by hardware selection on BS pins.The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CS#	D/C#	RES#
BS=L 4-wire SPI	SDA	SCL	CS#	D/C#	RES#
BS=H 3-wire SPI	SDA	SCL	CS#	L	RES#

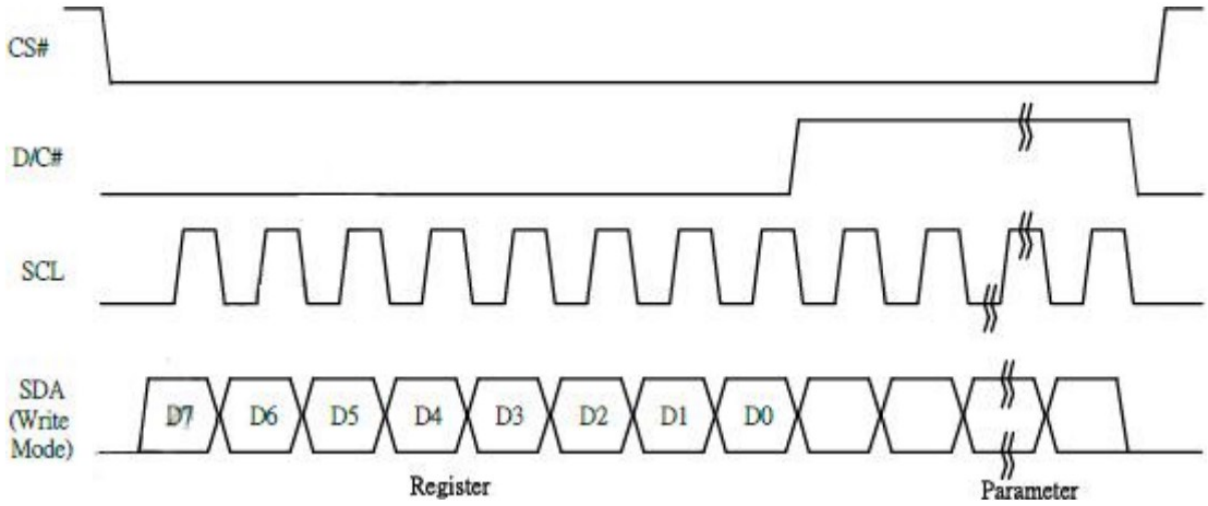
6.3.2 MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#.
In 4-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN.

Function	CS#	D/C#	SCL
Write command	L	L	↑
Write data	L	H	↑

Note:
(1) ↑ stands for rising edge of signal

SDA is shifted into an 8-bit shift register in the order of D7，D6，…D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/ Data Byte register or command Byte register according to D/C# pin.



Write procedure in 4-wire SPI mode

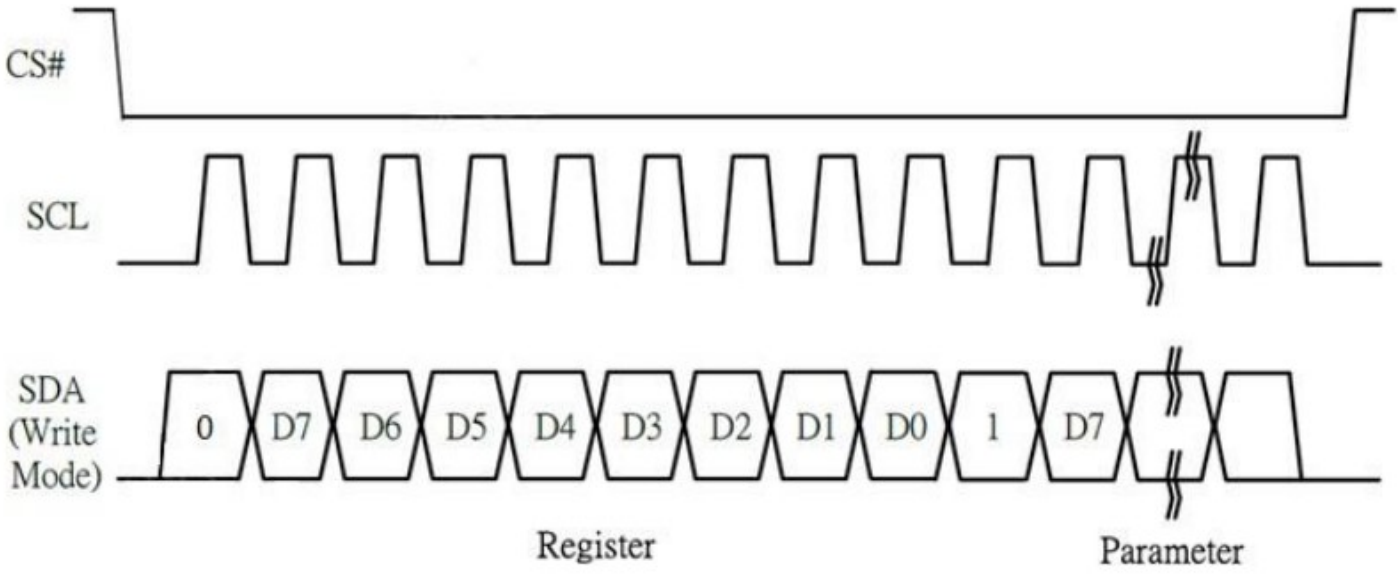
6.3.3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial SCL，serial data SDA and CS#. In 3-wire SPI mode，D0 acts as SCL ,D1 acts as SDA，The pin D/C# can be connected to an external ground. The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit , D/C bit, D7 to D0 bit，The D/C# bit (first bit of the sequential data)will determine the following data byte in shift register is written to the Display Data RAM(D/C# bit =1) or the command register (D/C# bit = 0). Under serial mode , only write operations areallowed.

Under serial mode, only write operations are allowed.

Function	CS#	D/C#	SCLK
Write command	L	Tie LOW	↑
Write data	L	Tie LOW	↑

Note: ↑ stands for rising edge of signal



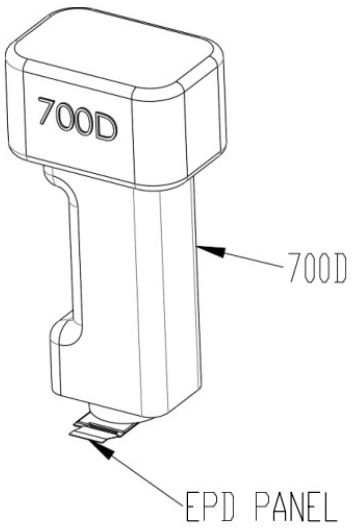
Write procedure in 3-wire SPI mode

7. Optical Characteristics

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified

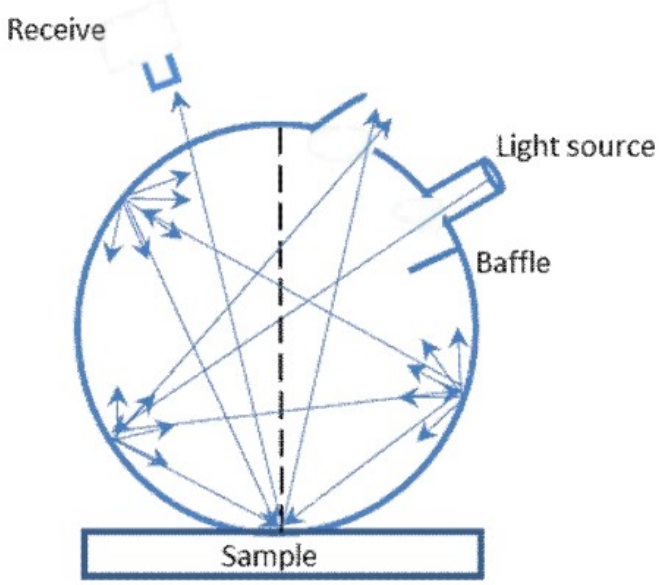
Item	Color	Symbol	Rating			Units	Notes
			Min.	Typ.	Max.		
Contrast ratio	White/Black	CR	-	20:1	-	-	θx=θy=0 (1),(2),(5),(6)
Refresh time	Black/ White/ Red	Tr		22		sec	(1),(3),(4),(6)
White state	White	L*		65	-	-	θx=θy=0 (1),(2),(6)
	White	a		-0.3			
	White	b*		0.74	-		
Red state	Red	L*	-	25	-		θx=θy=0 (1),(2),(6)
	Red	a*		37			
	Red	b*		22			
Reflectance	White	R%		37			(1),(2),(6)

Note (1): Panel is driven by SID waveform without masking film and optical measurement by ” 700D” with D65 light source and SCE mode.

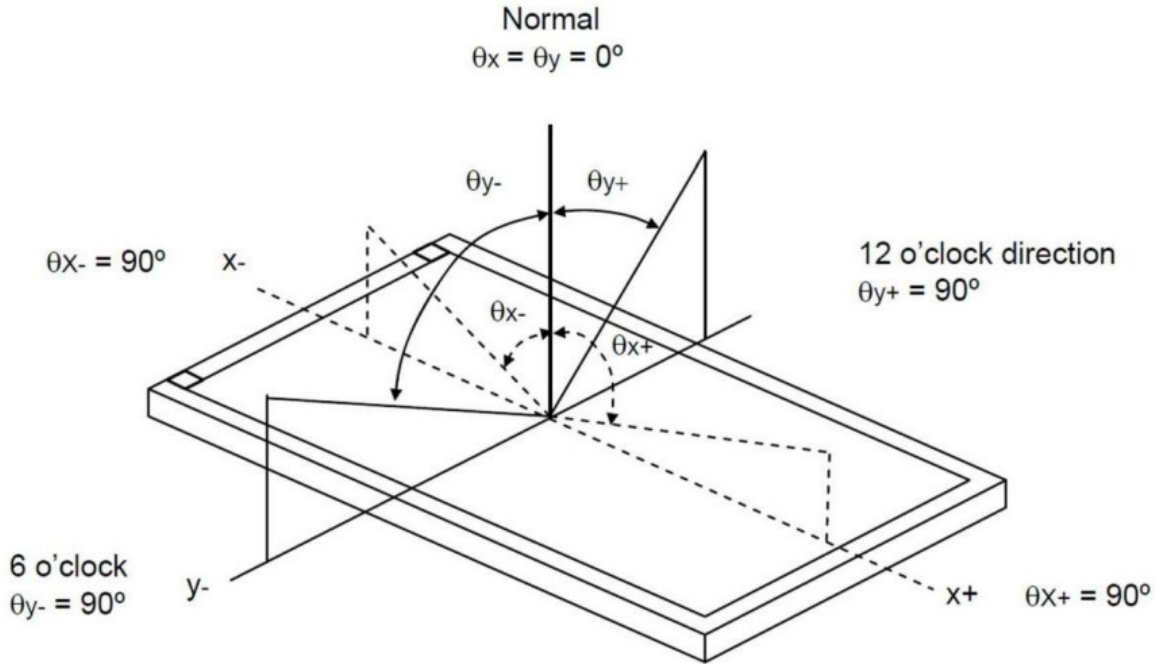


Optical measurement

SCE mode



Note (2): Definition of Viewing Angle (x, y)



Definition of Viewing Angle to Measure Contrast Ratio

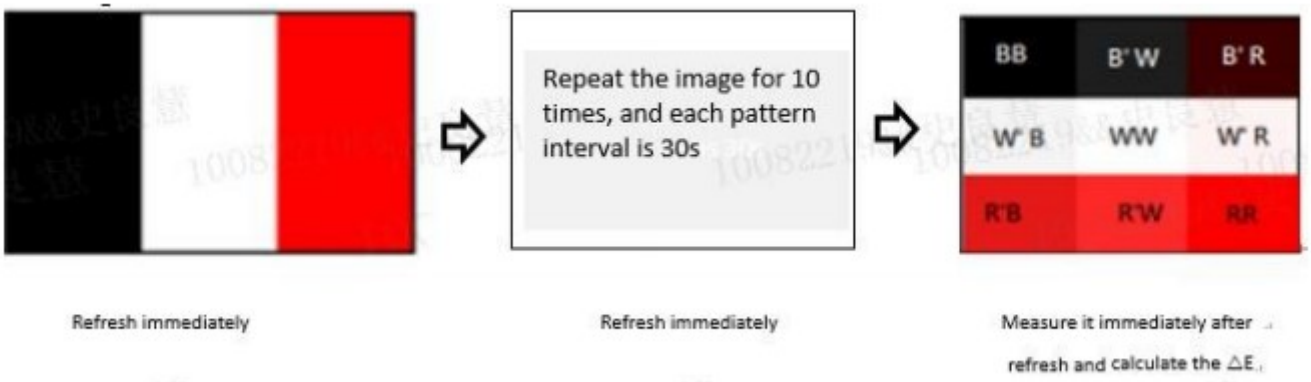
Note (3): Refresh time is the time that e-paper particles move not including the power on and off time. The refresh time is measured at 25 °C. The refresh time and contrast ratio varies due to different films,display
performance requirements, and ambient temperatures.

Note (4): Tr is the refresh time for an image which has no Red. For an image with Red, Red/White, Red/Black, or Red/Black/White, the total update time is (Tr).

Note (5): Contrast ratio (C.R.): The Contrast ratio is calculated by the following expression.
C.R. =(R%White)/(R% Black).

Note (6): Optical data is measured at 60 seconds after refresh with SID’s global update procedure

Below are test method to verify if ghosting is within an acceptable range. The measured data (L*, a*, b*) tocalculate color different, △E00 (CIEDE 2000).The condition of measurement is to follow “Table 7-1 Optical Measurement Conditions“ Ghosting Measurement



Item	Rating		
	Min.	Typ.	Max.
B’W△E00	-	-	2
W’B△E00	-	-	2
R’W△E00	-	-	2
W’R△E00	-	-	2
B’R△E00	-	-	2
R’B△E00	-	-	2

8. Handling, Safety and Environment Requirements

1. The EPD Panel / Module is manufactured from fragile materials such as glass and plastic, and may be broken or cracked if dropped. Please handle with care. Do not apply force such as bending or twisting to the EPD panel
2. The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
3. Do not apply pressure to the EPD panel in order to prevent damaging it
4. Do not connect or disconnect the interface connector while the EPD panel is in operation
5. Do not stack the EPD panels / Modules.
6. Keep the EPD Panel / Module in the specified environment and original packing boxes whenstorage in order to avoid scratching and keep original performance.
7. Do not disassemble or reassemble the EPD panel
8. Use a soft dry cloth without chemicals for cleaning. Please don't press hard for cleaning because the surface of the protection sheet film is very soft and without hard coating. This behavior would make dent or scratch on protection sheet
9. Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation
10. It's low temperature operation product. Please be mindful the temperature different to make frost or dew on the surface of EPD panel. Moisture may penetrate into the EPD panel because of frost or dew on surface of EPD panel, and makes EPD panel damage.
11. High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time. Please store the EPD panel in controllable environment of warehouse and original package. Without sunlight, without condensation a temperature range of 15ºC to 35ºC, and humidity from 30%RH to 60%RH.

9. Reliability test

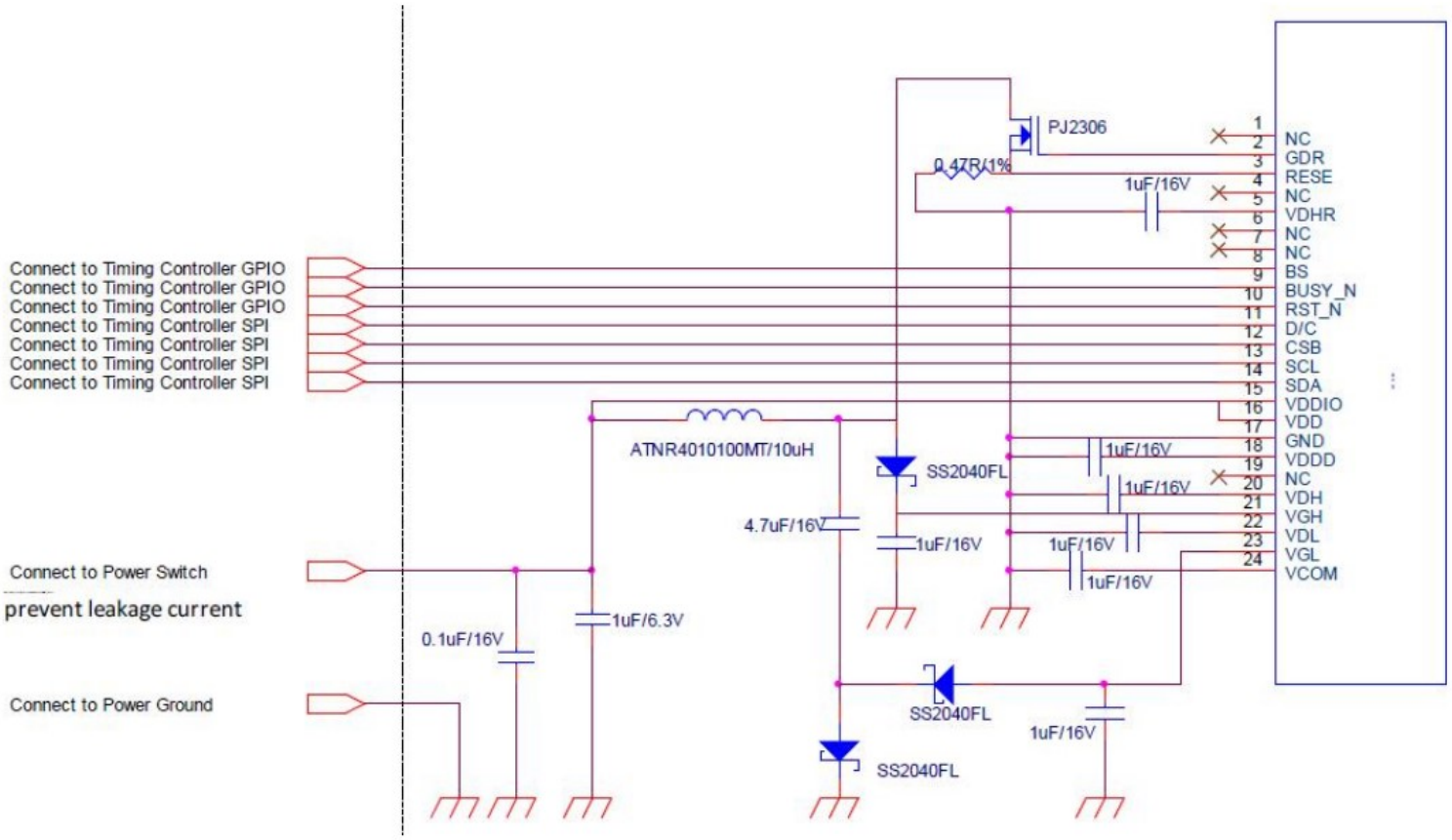
Item	Test Condition	Remark
Low Temperature Operation	0 ℃ for 240h	(1) (2)
High Temperature/Humidity Operation	40 ℃ / 70 %RH for 240h	(1) (2)
High Temperature Storage	60 ℃ / 40 %RH for 240h	(1)(2)(3)
Low Temperature Storage	-20 ℃ for 240h	(1)(2)(3)
High Temperature/Humidity Storage	50 ℃ / 80 %RH for 240h	(1)(2)(3)
Thermal Cycles (Non-operation)	1 Cycle:-20℃/30min → 60℃/30min, for 100 Cycles	(1)(2)(3)
Package Drop Test	Drop from 97cm. (ISTA) 1 corner, 3 edges, 6 sides. One drop for each.	(1)(2)(3)
Package Random VibrationTest	1.15Grms, 1Hz ~ 200Hz. (ISTA)	(1)(2)(3)

Note (1): No condensation and no frost during test. End of test, function, mechanical, and optical shall besatisfied.

Note (2): The test result and judgment are based on OTP driving waveform.

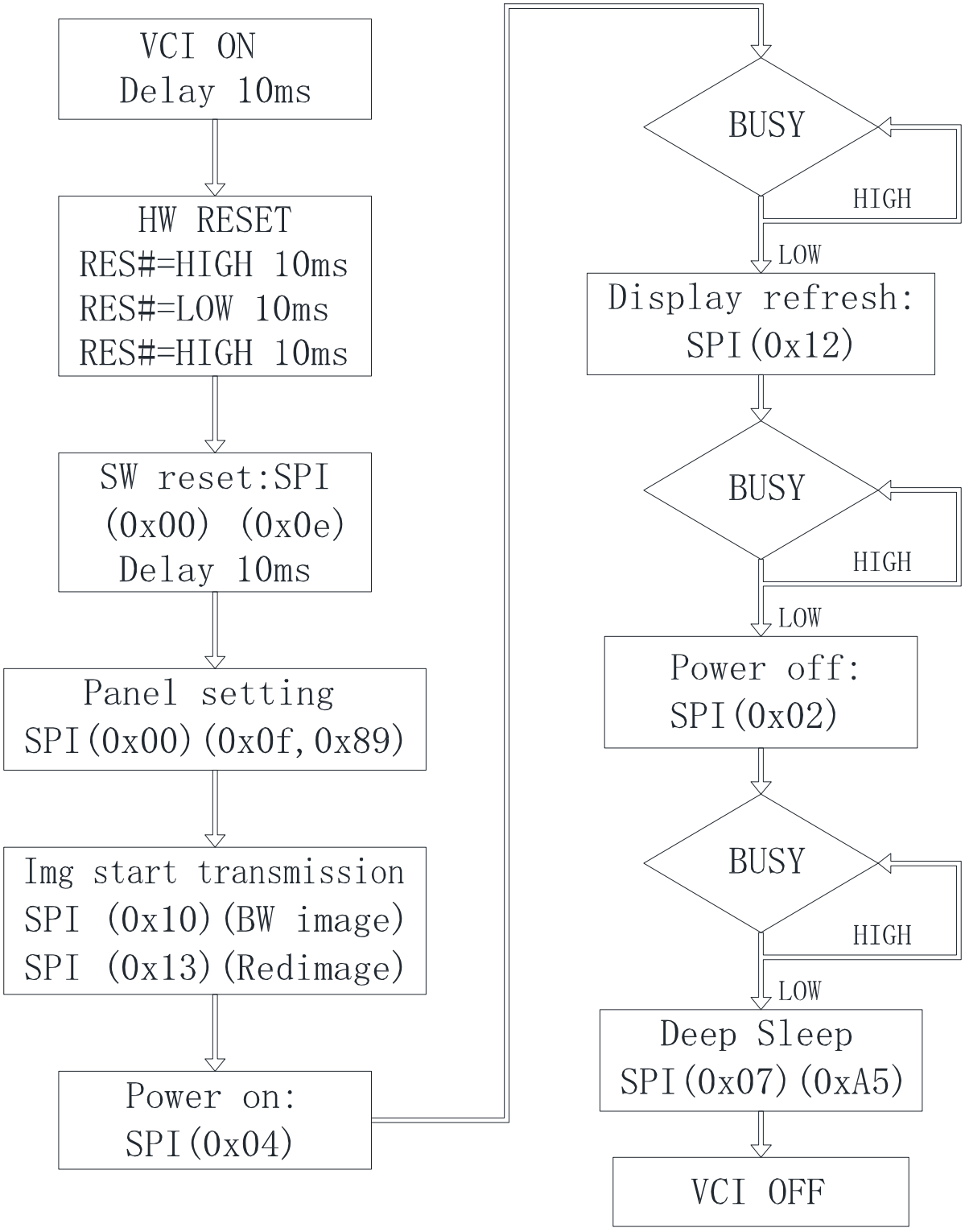
Note (3):Stay white pattern for storage and non-operation test.

10. Typical Application Circuit with SPI Interface



Type	Part	Vendor
Inductor	10uH ATNR4010100MT +-20% 0.8A	ARLITECH
Transistor	PJ2306 SOT-23 N-Channel 30V/3.2A	PANJIT
Diode	SS2040FL SOD-123FL	PANJIT

11. Typical Operating Sequence



12. Inspection condition

12.1 Environment

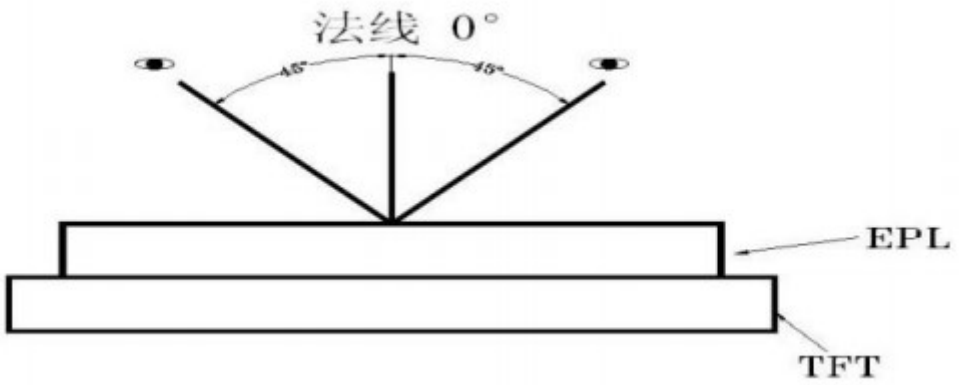
Temperature： 25±3 ℃

Humidity：55±10%RH

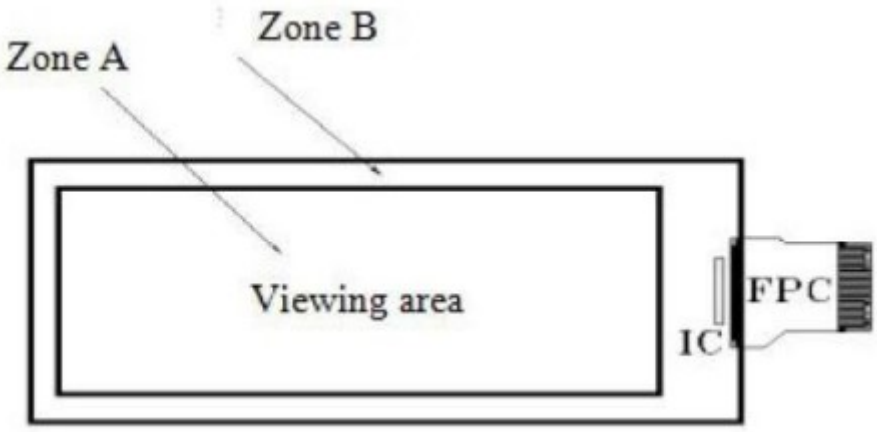
12.2 Illuminance

Brightness:1200～1500LUX; distance: 30CM; Angle: Relate 45°surround.

12.3 Inspect method

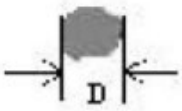
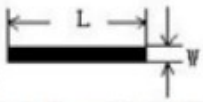


12.4 Display area

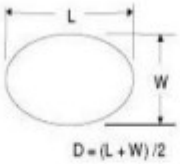
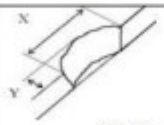
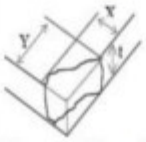
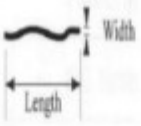


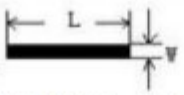
12.5 Inspection standard

12.5.1 Electric inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	Display	Clear display Display complete Display uniform	MA	Visual inspection	Zone A
2	Black/White spots	 D≤0.3mm，Allowed 0.3mm＜D≤0.5mm。N≤3， 0.5mm＜D Not Allow	MI		
3	Black/White spots (No switch)	 L≤1.0mm,W≤0.15mm negligible 1.0mm＜L≤4.0mm 0.15mm＜W≤0.5mm N≤4 allowable L＞4.0mm ,W＞0.5mm is not allowed		Visual/ Inspection card	
4	Ghost image	Allowed in switching process	MI	Visual inspection	
5	Flash dot / Multilateral	Flash points are allowed when switching screens Multilateral colors outside the frame are allowed for fixed screen time	MI	Visual/ Inspection card	Zone A Zone B
6	Segmented display	Selection segments are all displayed, and other segments are not displayed after the selection segment.	MA	Visual inspection	Zone A
7	Short circuit/ Circuit break/ Abnormal Display	Not Allow			

12.5.2 Appearance inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 D≤0.3mm，Allowed 0.3mm＜D≤0.5mm，N≤5 D＞0.5mm，Not Allow	MI	Visual inspection	Zone A
2	Glass crack	Not Allow	MA	Visual / Microscope	Zone A Zone B
3	\Dirty	Allowed if can be removed	MI		Zone A Zone B
4	Chips/Scratch/ Edge crown	 X≤3mm,Y≤0.5mm  2mm≤X or 2mm≤Y Allow  W≤0.1mm,L≤5mm, n≤ 2 Edge crown：X≤0.3mm，Y≤3mm	MI	Visual / Microscope	Zone A Zone B
5	TFT Cracks	 Not Allow	MA	Visual / Microscope	Zone A Zone B
6	Dirty/ foreign body	Allowed if can be removed/ allow	MI	Visual / Microscope	Zone A / Zone B
7	FPC broken/ FPC oxidation / scratch	  Not Allow	MA	Visual / Microscope	Zone B

8	B/W Line	 L≤1.0mm,W≤0.15mm negligible 1.0mm<L≤4.0mm 0.15mm<W≤0.5mm N≤4 allowable L>4.0mm ,W>0.5mm is not allowed	MI	Visual / Ruler	Zone B
9	TFT edge bulge /TFT chromatic aberration	TFT edge bulge: X≤3mm，Y≤0.3mm Allowed TFT chromatic aberration :Allowed	MI	Visual / Microscope	Zone A Zone B
10	Electrostatic point	D≤0.25mm, allow 0.25mm<D≤0.4mm ,n≤4 allow D>0.4mm is not allowed (n≤8 items are allowed within 5 mm in diameter)	MI	Visual / Microscope	Zone A
11	PCB damaged/ Poor welding/ Curl	PCB（Circuit area）damaged Not Allow PCB Poor welding Not Allow PCB Curl≤1%	MI	Visual / Ruler	Zone B
12	Edge glue height/ Edge glue bubble	Edge Adhesives H≤PS surface (Including protect film) Edge adhesives seep in≤1/2 Margin width Length excluding Edge adhesives bubble：bubble Width ≤1/2 Margin width；Length ≤0.5mm。n≤5	MI		
13	Protect film	Surface scratch but not effect protect function, Allow	MI	Visual Inspection	Zone B
14	Silicon glue	Thickness ≤ PS surface(With protect film): Full cover the IC; Shape: The width on the FPC ≤ 0.5mm (Front) The width on the FPC≤1.0mm (Back) smooth surface, No obvious raised.	MI	Visual Inspection	
15	Warp degree (TFT substrate)	 t≤1.5mm	MI	Ruler	
16	Color difference in COM area (Silver point area)	Allowed		Visual Inspection	

13. Packaging